AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring level in parallel along a peripheral portion of a chip within an inner region of the chip;

a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot without being connected to the first I/O slot;

a second pad arranged on a wiring level different from said first I/O slot and arranged apart from the peripheral portion of the chip as compared with the first pad;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned ~~in~~ at the peripheral portion of the inner region of the chip above the first I/O slot;

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot; and

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot.

2. (Canceled)

3. (Canceled)

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4. (Canceled)

5. (Canceled)

6. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the first and second I/O slots, the first and second pads and the first wiring and the second wiring are each designed and fixed in advance.

7. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are the same in wiring level.

8. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the first wiring and the second wiring are arranged in an uppermost layer of the chip.

9. (Canceled)

10. (Previously Presented) The semiconductor integrated circuit device according to claim 1, further comprising a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot, wherein the third wiring is isolated from the second wiring, and the fourth wiring is isolated from the first wiring.

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

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15. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the I/O slot different from the first I/O slot is the second I/O slot.

16. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the first and second pads are arranged on the same wiring level.

17. (Previously Presented) The semiconductor integrated circuit device according to claim 1, wherein the first and second I/O slots are adjacent to each other.

18. (Previously Presented) The semiconductor integrated circuit device according to claim 1, further comprising a fourth wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the second wiring to the first I/O slot.

19. (Previously Presented) The semiconductor integrated circuit device according to claim 18, wherein the third wiring and the fourth wiring do not overlap.

20. (Previously Presented) The semiconductor integrated circuit device according to claim 18, wherein the fourth wiring is shorter than the third wiring.

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